INTEGRATED CIRCUIT MEMORY DEVICES HAVING ASYNCHRONOUS FLOW-THROUGH CAPABILITY

Abstract of the Disclosure

Asynchronous memory devices utilize preferred loopback operations to provide efficient and high speed "flow-through" of write data when conventional flow-through operations are not available. An integrated circuit memory device includes a memory array having first and second ports that can each support asynchronous read and write access and a first input/output control circuit. The first input/output control circuit is electrically coupled to the first port and includes a first sense amplifier configured to receive read data from the first port and a first bypass latch having an output coupled to the first sense amplifier. A second input/output control circuit is also provided. The second input/output control circuit is electrically coupled to the second port and includes a second sense amplifier, configured to receive read data from the second port, and a second bypass latch. The second bypass latch has an output coupled to the second sense amplifier and an input coupled to receive write data directly from the first input/output control circuit during a first-to-second flow-through mode. The first bypass latch also has an input coupled to receive write data directly from the second input/output control circuit during a second-to-first flow-through mode.

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